Phase Disposition PWM Technique for Eleven Level Cascaded Multilevel Inverter with Reduced Number of Carriers

G. Sridhar[1] P. Satish Kumar[2] M. Sushama[3]

Abstract– Applying pulse width modulation (PWM) techniques for cascaded multilevel inverters are very complex for topologies with reduced number of switches. In this paper phase disposition (PD) pulse width modulation technique is implemented with lesser carrier signals and implemented on eleven levels cascaded multilevel inverter under reduced switches topology. The required number of switching pulses generated by considering number of carrier signals is equal to number of switches instead of N-1 carrier signals. This technique allows lower switching transition and it leads to reduced switching losses for topologies utilize minimum number of switches. 1.2 KHz carrier frequency is used to generate switching pulses and verified up to 100 kHz. The Total harmonic distortion is observed for various switching frequencies. The obtained output voltage levels using PD PWM technique proved mathematically. The performance of proposed algorithm is evaluated using Matlab/Simulink.

Keywords– Cascaded Multilevel Inverters, Diagonal dc source, Phase Disposition (PD) PWM Technique.

I. INTRODUCTION

In recent years several topologies are presented for cascaded multilevel inverter under reducing switches concept, some of them are symmetrical and asymmetrical [1]-[10], The advantages of above all structures is the low variety of dc voltage sources, which is the most important feature in determining cost of the inverter [1],Multilevel converters have some particular disadvantages. They need a large number of power semiconductor switches, which increase the cost and control complexity and reduce the overall reliability and efficiency [2].To minimize above mentioned disadvantages number of voltage levels are increased with minimum dc voltage sources and switches. In multilevel inverters the power quality is improved as the number of levels increases at the output voltage and can sustain the operation in case of internal fault [4].Using series and parallel operation of dc voltage sources for eleven levels of output voltage topology presented in [5] utilizes 10switches and 3 dc voltage sources and bus voltage THD is 13.1% but with the topology presented in figure1, 11 voltage levels are obtained using only 9switches and 2 dc voltage sources, therefore the topology presented in Fig1 is smaller because the number of switching devices are reduced .

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[1] **Department of Electrical Engineering, Jyothishmathi Institute of Technology and Science, Karimnagar**
E-mail: gaddamsridhar78@gmail.com
[2] **Electrical Engineering Department Osmania University, E-mail: satish_8020@yahoo.co.in**
[3] **Electrical and Electronics Department, JNTUH, Hyderabad.**
Email: m73sushama@yahoo.co.in

PV cells, batteries, capacitors etc. can be used as voltage sources for the presented diagonal dc source cascaded MLI,

The phase disposition technique produces fewer harmonic because it puts harmonic energy directly into a common mode carrier component which cancels across line to line output [6].

In this paper Phase disposition modulation technique is implemented with new algorithm to generate switching pulses to turn on S1, S2, S3, S4, S5 which connects dc voltage sources in series and parallel and the output voltage collected across RL load. In the proposed phase disposition algorithm N-6 carrier signals(equal to switches present in polarity generation circuit) are taken and are compared with sinusoidal reference to achieve gate pulses for generating eleven levels output. It allows lower switching transitions leads to reduced losses in the circuit. The total harmonic distortion observed for varying switching frequencies from1.2kHz to 100 kHz.

II. DIAGONAL DC SOURCE CASCADED MULTI LEVEL INVERTER

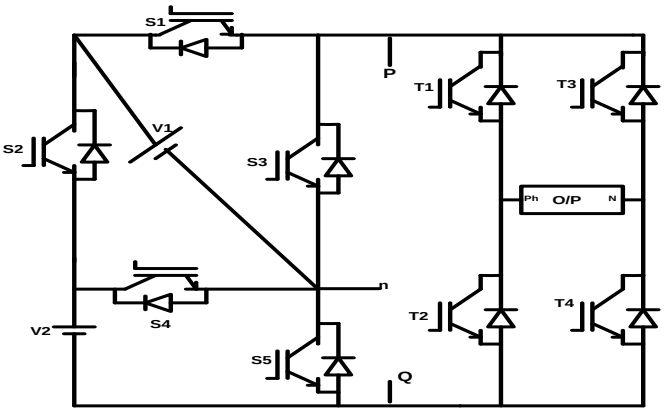

Fig1. Diagonal DC Source Cascaded MLI

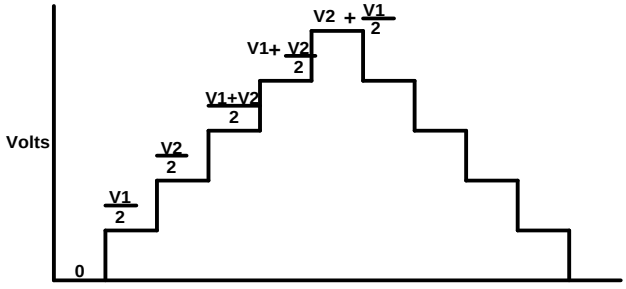

Fig2.Output Voltage across PQ

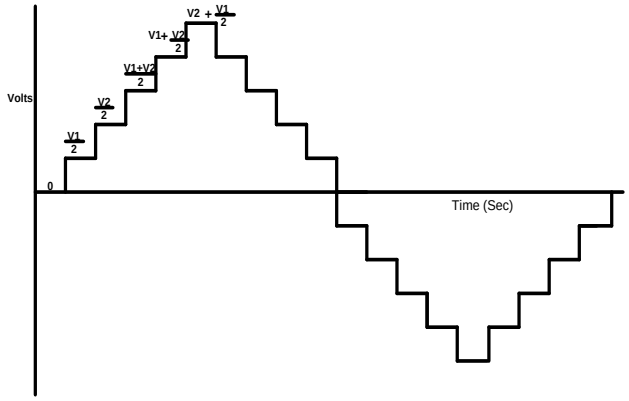

Fig3. Output Voltage across Load

The diagonal dc source cascaded multilevel inverter consist of two circuits (i) Polarity generation is used for generating only positive voltage levels as shown in Fig2. (ii) Polarity conversion circuit is used for converting positive polarity into both positive and negative polarity voltage levels. The output of the polarity conversion circuit is shown in Fig3.
The operation of diagonal dc source cascaded MLI divided into six modes i.e. mode0, mode1, mode2, mode3, mode4, mode5, the switching sequence in every mode and corresponding voltages listed in Table I. The major advantage with the algorithm applied in phase disposition pwm is that the selected switching sequence allows half of the applied voltages across polarity generation circuit, this gives reduced voltage stresses across the switches.

Table 1: Switching Sequence for Eleven Level Diagonal Dc Source Cascaded MLI

Level / Mode	0	1	2	3	4	5
1	**S3, S5**	**S1,S3 ,S5**	**S1,S2, S3 ,S5**	**S1,S2,S5**	**S1,S2,S4 , S5**	**S1,S2,S4**
Output Voltage (Volts)	0	$\frac{V1}{2}$	$\frac{V2}{2}$	$\frac{V1+V2}{2}$	$V1+\frac{V2}{2}$	$\frac{V1}{2}+V2$

III. Mathematical Analysis Of Diagonal DC source Cascaded Mli

During each mode of operation the expected output voltages are calculated by taking each switch resistance 1mΩ using Kirchhoff's laws.

Mode0: When s3 and s5 are switched on the voltage across PQ

$$Vpq = 0 \tag{1}$$

Mode1: When the switches s1, s3, and s5 are turned on the following equations can be written

$$i_1x + i_2x + \ldots..i_nx = V_1 \tag{2}$$

$$i_1x = i_2x = ia \tag{3}$$

$$i_a = \frac{V_1}{2} \tag{4}$$

During this interval the voltage available across Pn is $\frac{V_1}{2}$

Mode2: When s1, s2, s3 and s5are switched on the following ***equation can be written***

$$i_1x + i_2x + ..inx = V_1 \tag{5}$$

$$i_1x = i_2x = i_b \tag{6}$$

$$i_b = \frac{V_1}{2} \tag{7}$$

The voltage present across Pn is $\frac{V_1}{2}$ *and*

$$i_3x + i_4x + \ldots i_nx = V_2 - V_1 \tag{8}$$

$$i_3x = i_4x = ic \tag{9}$$

$$i_c = \frac{V_2 - V_1}{2} \tag{10}$$

From above equation the voltage present across PQ is

$$V_P n + Vn_Q = \frac{V_1}{2} + \frac{V_2 - V_1}{2} = \frac{V_2}{2} \tag{11}$$

Mode4: When switches s1, s2 and s5 are switched on, the following equation can be written

$$i_5x + i_6x + \ldots i_nx = V_2 - V_1 \tag{12}$$

$$i_5x = i_6x = i_d \tag{13}$$

$$i_d = \frac{V_2 - V_1}{2} \tag{14}$$

The voltage present across PQ is

$$V_1 + \frac{V_2 - V_1}{2} = \frac{V_1 + V_2}{2} \tag{15}$$

Mode5: When switches s1, s2, s4, and s5 are switched on

$$2i_7x + i_8x = V_1 \tag{16}$$

$$i_7x + 2i_8x = V_2 \tag{17}$$

Solving above equation we get voltage across PQ is

$$V_{PQ} = V_1 + \frac{V_2}{2} \tag{18}$$

Mode6: when s1,s2 and s4 are turned on the voltage across PQ is

$$V_{PQ} = \frac{V_1}{2} + V_2 \tag{19}$$

where *i1x, i2x, i3x ,…inx* are respective loop currents, *V1,V2, …Vn* voltages applied across respective cell

IV. Proposed Phase Disposition PWM technique Algorithm

In this paper the target is to generate switching pulses for switches S1, S2, S3, and S4and S5 shown in Fig1 at the desired time intervals. First time attempt was made to generate switching pulses using phase disposition pulse width modulation technique, an algorithm is proposed for reducing switches topologies.

In Phase disposition PWM technique N-1 carrier waves are used to generate N level output in conventional cascaded H bridge topologies. But with the proposed algorithm for generation of eleven level cascaded MLI under reduced switches topology the number of triangular carrier signals are equal to number of switches in polarity generation circuit, for generating eleven level only five triangular carrier signals are used.

Five triangular carrier signals are compared with sinusoidal reference signal at their respective time of intervals as shown in Fig4. The selection of triangular carrier frequency plays key role for obtaining required width of pulses. The generated pulses shown in Fig5.This technique greatly reduce the complexity in PWM circuit because of less number of carriers.

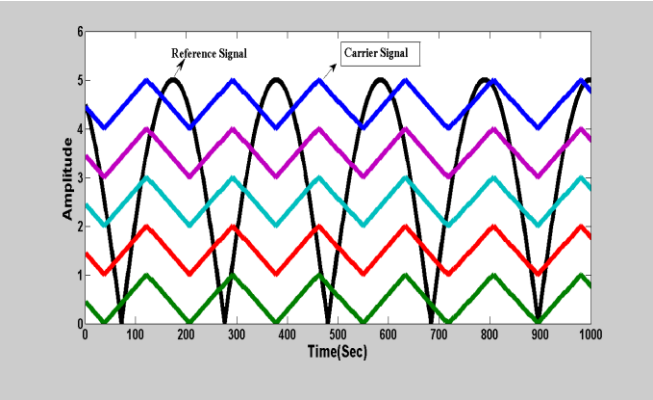

Fig4. Reference and carrier signals in Proposed Phase Disposition PWM Technique for Eleven level Diagonal DC source Cascaded MLI

V. Switching Pulses Generation with The Proposed Phase Disposition PWM Technique Algorithm

The design of the inverter is done using various factors; these factors are obtained from various parameters that contribute the efficiency of inverter

The switching frequency is estimated using frequency modulation index is given by $M_f = \frac{f_c}{f_r}$

where *fc* and *fr* are carrier wave and reference wave frequency.

The amplitude modulation index is defined as

$$M = \frac{V_m}{(n-1)Vc}$$

where the *Vm* peak to peak value of the reference wave and *Vc* are the amplitude of the carrier wave.

The THD is measured as the ratio of all the harmonics in a switching system to the fundamental unit.

$$THD = \frac{\sqrt{\sum_{i=2}^{n} A_i}}{A}$$

where, Ai is the i[th] voltage/current harmonic value. Pulse width modulated systems are usually characterized with power and harmonic losses which result from the switching and conduction losses of the switches/transistors/thyristors that are sed. The losses in the modulation techniques cause the average reduction in phase-phase voltages at each switching frequencies [12].

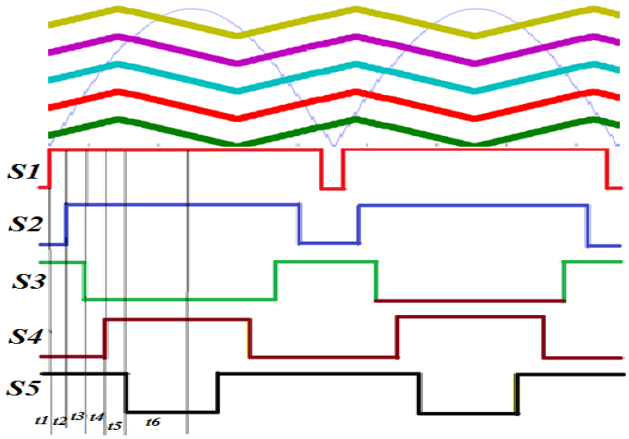

Fig5. Switching Pulses in Proposed Phase Disposition PWM Technique

During each switching interval the magnitude of voltages present across PQ is represented below.

$$0 \le t \le t_1 = 0\ Volts$$

Switches S3, S5 are turned ON

$$t_1 \le t \le t_2 = \frac{V_1}{2}\ Volts$$

Switches S1, S3, S5 are turned ON

$$t_2 \le t \le t_3 = \frac{V_2}{2}\ Volts$$

Switches S1, S2, S3, and S5 are turned ON

$$t_3 \le t \le t_4 = \frac{V_1 + V_2}{2}\ Volts$$

Switches S1, S2, S5 are turned ON

$$t_4 \le t \le t_5 = V_1 + \frac{V_2}{2}\ Volts$$

Switches S1, S2, S4, and S5 are switched ON

$$t_5 \le t \le t_6 = \frac{V_1}{2} + V_2\ Volts$$

Switches S1, S2, S4 are switched ON

The above obtained voltage magnitudes during each interval are verified mathematically in section III and obtained voltage magnitudes matching with the simulated results.

VI. Simulation Circuit

The diagonal dc source cascaded multilevel inverter circuit shown in Fig1. To generate switching pulses Phase disposition PWM technique is employed. For generating required number of switching pulses under proposed algorithm the below Matlab/Simulink circuit is designed. To

generate five switching pulses, five carrier signals compared with the positive peak of the sinusoidal signal. All carrier signals switching frequency is selected as 1.2 kHz and 50 Hz reference signal is compared with the carrier signals as shown in Fig6. The wave forms observed for a modulation index unity.

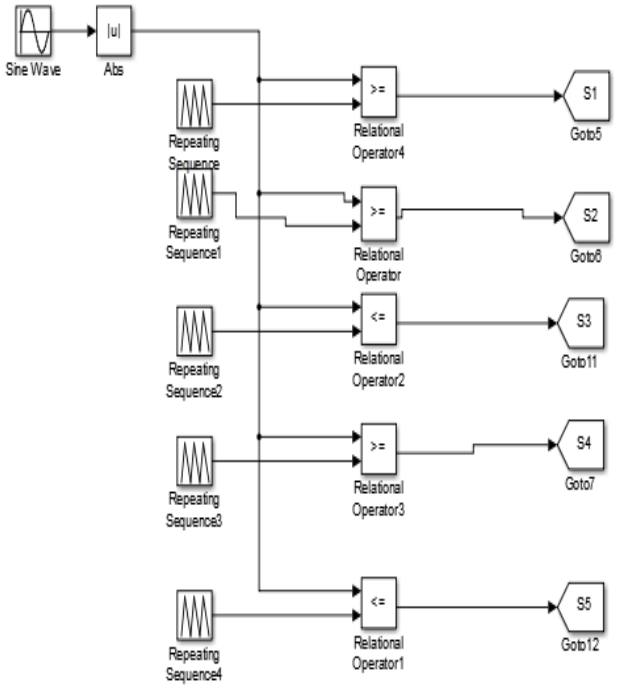

Fig6. Phase Disposition PWM Circuit for generating switching pulses with the proposed algorithm

VII. Simulation Results

The proposed algorithm for Phase Disposition PWM technique simulated using Matlab /Simulink R2013 version. For observing proposed algorithm to generate required switching pulses eleven level diagonal dc source cascaded multilevel inverter is considered with RL load as R=45Ω and L=55mH. It was observed that with the proposed algorithm the THD is reduced. For the voltage wave the THD is 14,21% and the current THD is 9.66%. It is observed that the voltage THD is slightly increasing with the switching frequency at 100 kHz and the current THD is reducing with the switching frequency at 100 kHz switching frequency its value is only 0.73%. Results obtained with proposed algorithm are shown with their THD in Fig7, Fig8, Fig9 and Fig10.

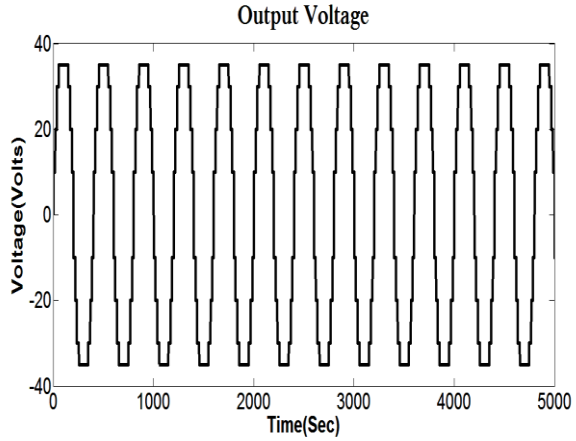

Fig7. 11 level Output voltage with proposed Phase Disposition (PD) algorithm

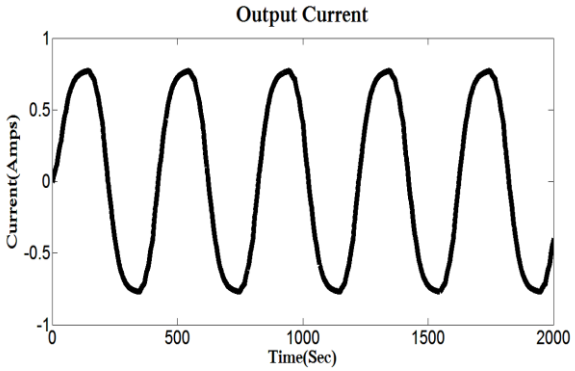

Fig8. Output Current with proposed Phase Disposition (PD) algorithm

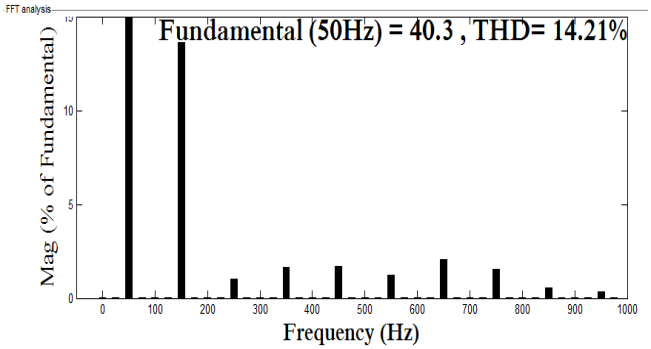

Fig9. 11 level Output voltage THD with proposed Phase Disposition (PD) algorithm

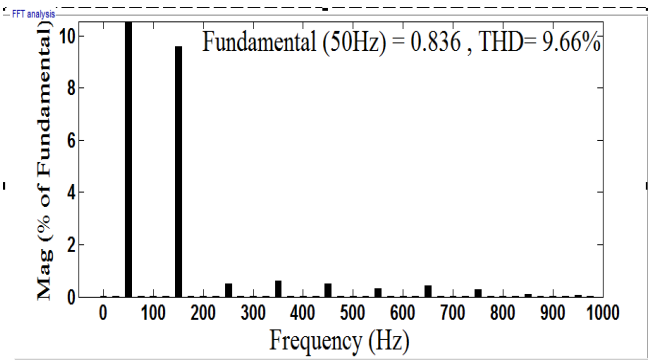

Fig8. Output Current THD with proposed Phase Disposition (PD) algorithm

VIII. Conclusion

In this paper new algorithm was proposed to Phase Disposition PWM technique and implemented on diagonal dc source cascaded multilevel inverter under reduced switches topology and it was verified for switching frequencies of 1.2kHz, 5kHz, 10kHz and 100kHz at unity modulation index using Matlab/Simulink. The proposed modulation technique increase the number of levels with reduction of carrier signals. In the future the Simulink results are verified with hardware prototype.

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BIOGRAPHIES

G.Sridhar was born in Karimnagar, Telangana, India in 1978. He obtained B.Tech degree in Electrical Engineering from University of Madras in 2000 and M.Tech in Power Systems with emphasis on High Voltage Engineering in 2005from JNTU Kakinada. He is pursing PhD degree in the area of multilevel inverter. He is working as associate professor in the department of Electrical Engineering. Jyothishmathi institute of technology and science, karimnagar. His research interest includes power electronics and multilevel inverters and has 17 years of teaching experience.

P. Satish Kumar was born in Karimnagar, Andhra Pradesh, INDIA in 1974. He obtained the B.Tech. degree in Electrical and Electronics Engineering from JNTU College of Engineering, Kakinada, INDIA in 1996. He obtained M.Tech degree in Power Electronics in 2003 and Ph.D. in 2011 from JNTUH, Hyderabad. He has more than 19 years of teaching experience and at present he is an Assistant Professor in the Department of Electrical Engineering, University College of Engineering, Osmania University, and Hyderabad, INDIA. His research interests include Power Electronics, Special Machines, Drives and Multilevel inverters and guiding seven research scholars. He presented many research papers in various national and international conferences and published many papers in various international journals. He is the Editorial Board member of many international journals. At present he is actively engaging in two Research Projects in the area of multilevel inverters funded by University Grants Commission (UGC), New Delhi, and Science and Engineering Research Board (SERB), New Delhi. India. He received "Best Young Teacher Award-2014" from the state Government of Telangana. He also received the "Award for Research Excellence". He is guiding 8 PhD scholars in the area of power electronics and drives.

M.Sushama was born in 1973, in Nalgonda district, Telangana state. India. Obtained B.Tech degree in 1993 and M.Tech degree in 2003, specialization in Electrical Power Systems from JNTU, INDIA. She obtained her Ph.D. from JNTU Hyderabad, in 2009 in the area of "Power Quality" using Wavelet Transforms. She has more than 22 years of teaching experience and at present she is working as head and professor in the department of electrical and electronics engineering, JNTUH, Hyderabad, India. Her research interests includes green energy, power systems, power electronics, facts controllers and power quality and harmonics.